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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,089	11/25/2003	Myoen-Song Choi	4366-032255	7157

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EXAMINER	
LE, TOAN M	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/722,089	CHOI ET AL.	
	Examiner	Art Unit	
	Toan M. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-4 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,756,786 (Choi et al.) in view of Saha et al. (U.S. Patent No. 6,476,613).

U.S. Patent No. 6,756,786

1. A method for detecting a line-to-ground fault location in a power network comprising the steps of:

determining elements of a line impedance matrix and phase voltage and current at a relay;

determining a line-to-ground fault distance d by substituting said elements of said line impedance matrix, said phase voltage and current into a fault location equation based on direct circuit analysis;

wherein said fault location equation is derived from a model consisting of said phase voltage and current at the relay, a fault current, a fault resistance and the line-to-ground fault distance;

wherein the model is described by the equation:

$V_{Sab} = (1\text{-}d) \times Zl_{abc} \times I_{Sabc} + V_{fabc}$,

where, $V_{Sabc} = [V_{Sa}\ V_{Sb}\ V_{Sc}]$: phase voltage vector, $I_{Sabc} = [I_{Sa}\ I_{Sb}\ I_{Sc}]$: phase current vector, $V_{fabc} = [V_{fa}\ V_{fb}\ V_{fc}]$: phase voltage vector at the fault location,

$$Zl_{abc} = \begin{bmatrix} Zl_{aa} & Zl_{ab} & Zl_{ac} \\ Zl_{ba} & Zl_{bb} & Zl_{bc} \\ Zl_{ca} & Zl_{cb} & Zl_{cc} \end{bmatrix};$$

is line impedance matrix, I_f: fault current, 1-d: fault distance;

wherein said fault location equation is derived by using the matrix inverse lemma:

$(A^{-1} + BCD)^{-1} = A - AB(C^{-1} + DAB)^{-1}DA$, to simplify an inverse matrix calculation; and wherein the fault location equation is derived by direct circuit analysis without using the conventional symmetrical component transformation method.

2. The method of claim 1, wherein the power network is a 3-phase balanced network.

3. The method of claim 1, wherein the power network is a 3-phase unbalanced network.

4. The method of claim 1, wherein the fault location equation is derived by steps of:

(a) expressing the phase voltage of the a-phase which has the fault as follows:

$V_{Sa} = (1\text{-}d)(Zl_{aa}I_{Sa} + Zl_{ab}I_{Sb} + Zl_{ac}I_{Sc}) + I_f R_f$

(b) expressing the fault current I_f in terms of the phase current vector I_s by using current distribution law of a parallel network yielding:

$$\begin{bmatrix} I_f \\ 0 \\ 0 \end{bmatrix} = Y_f[Y_f + (dZl_{abc} + Zr_{abc})^{-1}]^{-1} \begin{bmatrix} I_{Sa} \\ I_{Sb} \\ I_{Sc} \end{bmatrix}; \quad Y_f = \begin{bmatrix} 1/R_f & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$Zr_{abc} = \begin{bmatrix} Zr_{aa} & Zr_{ab} & Zr_{ac} \\ Zr_{ba} & Zr_{bb} & Zr_{bc} \\ Zr_{ca} & Zr_{cb} & Zr_{cc} \end{bmatrix};$$

where Y_f is fault admittance matrix and Zr_{abc} is load impedance matrix;

(c) simplifying the equation of step (b) by using the inverse matrix lemma and substituting the simplified equation into the a-phase equation of step (a); and

(d) deriving a set of equations from a real and an imagery part of the equation obtained at step (c);

(e) deriving a second order polynomial equation by combining the set of equations obtained at step (d); and

(f) deriving the fault location equation by solving the second order polynomial equation.

Instant Application 10/722,089

1. A method for detecting a line-to-line fault location in a power network comprising the steps of:

determining elements of a line impedance matrix and a load impedance matrix, and phase voltages and currents at a relay;

determining a line-to-line fault distance d by substituting said elements of said line impedance matrix and said load impedance matrix, and said phase voltage and current into a fault location equation based on direct circuit analysis;

wherein said fault location equation is derived from a model consisting of said phase voltage and current at the relay, a fault current, a fault resistance and the line-to-line fault distance;

wherein the model is based on the line-to-line fault between a-phase and b-phase and described by a model equation:

$V_{Sa} - V_{Sb} = (1\text{-}d)((Zl_{aa} - Zl_{ba})I_{Sa} + (Zl_{ab} - Zl_{bb})I_{Sb} + (Zl_{ac} - Zl_{cb})I_{Sc}) + I_f R_f$,

where, $V_{Sabs} = [V_{Sa}\ V_{Sb}\ V_{Sc}]$: phase voltage vector, $I_{Sabc} = [I_{Sa}\ I_{Sb}\ I_{Sc}]$: phase current vector,

$$Zl_{abc} = \begin{bmatrix} Zl_{aa} & Zl_{ab} & Zl_{ac} \\ Zl_{ba} & Zl_{bb} & Zl_{bc} \\ Zl_{ca} & Zl_{cb} & Zl_{cc} \end{bmatrix};$$

is line impedance matrix, I_f: fault current, 1-d: fault distance;

wherein said fault location equation is derived by using the matrix inverse lemma:

$(A^{-1} + BCD)^{-1} = A - AB(C^{-1} + DAB)^{-1}DA$, to simplify an inverse matrix calculation; and wherein the fault location equation is derived by direct circuit analysis without using the conventional symmetrical component transformation method.

2. The method of claim 1, wherein the power network is a 3-phase balanced network.

3. The method of claim 1, wherein the power network is a 3-phase unbalanced network.

4. The method of claim 1, wherein the fault location equation is derived by steps of:

(a) expressing the fault current I_f in terms of the phase current vector I_s by using current distribution law of a parallel network yielding:

$$\begin{bmatrix} I_f \\ 0 \\ 0 \end{bmatrix} = Y_f[Y_f + (dZl_{abc} + Zr_{abc})^{-1}]^{-1} \begin{bmatrix} I_{Sa} \\ I_{Sb} \\ I_{Sc} \end{bmatrix}; \quad Y_f = \begin{bmatrix} 1/R_f & -1/R_f & 0 \\ -1/R_f & 1/R_f & 0 \\ 0 & 0 & 0 \end{bmatrix};$$

$$Zr_{abc} = \begin{bmatrix} Zr_{aa} & Zr_{ab} & Zr_{ac} \\ Zr_{ba} & Zr_{bb} & Zr_{bc} \\ Zr_{ca} & Zr_{cb} & Zr_{cc} \end{bmatrix};$$

where Y_f is fault admittance matrix and Zr_{abc} is load impedance matrix;

(b) simplifying the equation of step (a) by using the inverse matrix lemma and substituting the simplified equation into the model equation;

(c) deriving a second order polynomial equation with respect to the line-to-line fault distance d from a real or an imaginary part of the equation obtained at step (b); and

(d) deriving the fault location equation by solving the second order polynomial equation.

Choi et al. in '786 teach a method for detecting a line-to-ground fault location in a power network using a line impedance matrix, phase voltage and current at a relay, a line-to-ground fault distance based on a fault location equation model derived by using the matrix inverse.

Choi et al. do not mention detecting a line-to-line fault location in a power network using the method mentioned above.

Saha et al. teach a method for detecting a line-to-line fault location in a power network using a line impedance matrix, phase voltage and current at a relay, a line-to-line fault distance based on a fault location equation model using a line impedance matrix, phase voltage and current at a relay, a line-to-line fault distance based on a fault location equation model (col. 3, lines 60-67; col. 4, lines 1-67; col. 5, lines 1-50; equations 1-35).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have applied the method as described by Saha et al. into the method of Choi et al. in use of transmission links between power generation and energy consumption regions for accurate fault location estimation for three phase line using impedance matrices.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,198,746 to Gyugyi et al. U.S. Patent No. 5,072,403 to Johns

U.S. Patent No. 5,010,544 to Chang et al. U.S. Patent No. 4,719,580 to Nimmersjo

U.S. Patent No. 6,601,001 to Moore

A Fault Location Algorithm for Transmission Line Based on Distributed Parameter, Chen et al., IEEE 2001, Develop. in Power System Protection, Conf. Pub. No. 479, Pages 411-413

Fault Location Technique for Six Phase Transmission Lines With Unsynchronized Phasors, IEEE 1999, Pages 663-667

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

February 23, 2005

BRYAN BUI
PRIMARY EXAMINER